Memristor-Based Pattern Recognition for Image Processing: an Adaptive Coded Aperture Imaging and Sensing Opportunity

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ABSTRACT

Adaptive coded aperture (diffraction) sensing, an emerging technology enabling real-time, wide-area IR/visible sensing and imaging, could benefit from new high performance biologically inspired image processing architectures. The memristor, a novel two terminal passive device can enable significantly powerful biologically inspired processing architectures. This device was first theorized by Dr. Leon Chua in 1971. In 2008, HP Labs successfully fabricated the first memristor devices. Due to its unique properties, the memristor can be used to implement neuromorphic functions as its dynamics closely model those of a synapse, and can thus be utilized in biologically inspired processing architectures. This paper uses existing device models to determine how device parameters can be tuned for the memristor to be used in neuromorphic circuit design. Specifically, the relation between the different models and the number of states the device can hold are examined.

1. INTRODUCTION

The primate brain is significantly more powerful at recognizing images than existing image processing algorithms. At present there is significant interest in developing image processing architectures inspired by the organization of neural connections in the brain. Such architectures would be highly beneficial in adaptive coded aperture (diffraction) sensing. The recently discovered memristor could potentially enable significantly powerful biologically inspired neuromorphic image processing architectures. This device was first theorized by Dr. Leon Chua in 1971 as the fourth fundamental circuit element [1]. Similar to the resistor, capacitor, and inductor, the memristor is a two terminal passive device. The memristor also has the ability to change resistance as a function of voltage input, and the ability to retain a resistance value after the power source is no longer applied to the device. These features suggest that the memristor can be used to model a system similar to the synaptic response in brain tissue [2].

In 2008, Dr. Stanley Williams lead a research team at HP Labs to publish the first results of a fabricated memristor device [3]. The memristor device developed at HP Labs consists of two titanium oxide layers sandwiched between two platinum electrodes. One of the layers in the device was stoichiometric titanium dioxide (TiO2). The second layer was oxygen deficient titanium dioxide (TiO2-X). Since the oxygen deficiencies act as +2 charged dopants, the oxygen deficient layer is much more conductive than the TiO2 layer. Applying a voltage to the device causes the oxygen deficient layer to expand into the TiO2 layer, changing the resistance of the device. This can be visualized as a barrier between the titanium oxide layers changing position, determining the ratio of stochiometric titanium oxide to oxygen deficient titanium oxide. Since the mobility of the charges in the TiO2-X is so low, they tend to stay in the same position after the power is disconnected, resulting in a memory effect. The device is modeled as two resistors in series that have a resistance value determined by the position of the barrier between the TiO2 layer and the TiO2-X layer.

Memristors can be used to emulate the architecture of the brain within a size comparable to brain tissue. Also, the memristor behaves analogous to a synapse, the connection between two neurons. When one neuron fires a pulse to another, that pulse travels through the synapse connecting them. The synapse provides variable connection strength between neurons relative to how many pulses have passed through it. The value of connection strength stored in the synapse is closely modeled by the memristor’s ability to hold a time varying resistance.

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Since the discovery of the TiO$_2$ based memristors by HP Labs, a few institutions have fabricated devices for use in neuromorphic circuits, specifically [7, 8]. In [7] a silver chalcogenide device was fabricated at a total thickness of 130nm, and [8] discusses a device formed from a-Si and Ag. All of the devices can be modeled as a doped layer and an undoped layer sandwiched between two electrodes.

Neuromorphic systems would utilize memristors by using voltage pulses to vary the resistance of the device. The number of resistance levels in a device relates to numeric precision the device can provide. Since these devices can be made from a variety of different thicknesses and materials, the resistance levels in a memristor can be changed by varying device properties. If higher precision is needed by a neuromorphic system, multiple memristors could be utilized to represent a single synapse.

HP Labs released a memristor model in [3] that describes the charges in the doped layer to move with linear dopant drift. Since then, Joglekar and Wolf expanded on the model in [4] by defining a non-linear drift velocity. Furthermore, Zdenek Biolek et al. describe an alternative non-linear drift model for the memristor.

Previous studies examine the outputs of these models with sinusoidal input voltage. This does not show how many resistance levels a device can hold. This paper examines the three memristor models described above to compare the number of resistance levels they produce. More specifically, the models are tested to see how many different resistance levels can be reliably stored as a function of the device parameters.

Section 2 of this paper provides an analytical background to discuss the modeling equations provided by [3-6]. Section 3 discusses the parameters and inputs used to test the models. Section 4 presents simulation results generated by each of the models as well as the number of resistance levels each model can store as a function of the device parameters. Section 5 compares the data to the fabrication results in [7, 8], while section 6 concludes the paper.

### 2. ANALYTICAL BACKGROUND

The equations used to develop the memristor model were introduced in [3], with a more comprehensive analysis completed in [4]. HP labs described the I-V relationship for the TiO$_2$ memristor using equation (1). This equation states that the memristor can be modeled using two resistors in series where the resistance of each is dependent on $w(t)$, the thickness of the oxygen deficient, or doped layer. For analysis purposes, $w(t)$ can be seen as the position of a mobile barrier between the doped and undoped layers.

$$ V(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF} \left( 1 - \frac{w(t)}{D} \right) \right) I(t) $$  \hspace{1cm} (1)

According to [4], the drift velocity, $v_D$ of the charges in the oxygen deficient layer can be described using equation (2).

$$ \frac{dw}{dt} = v_D = \eta \mu_D \frac{R_{ON}}{D} I(t) $$  \hspace{1cm} (2)

where $\eta = \pm 1$ depending on the orientation of the memristor. If $\eta = 1$, then the width of the oxygen deficient layer will expand under positive bias, otherwise it will contract. $\mu_D$ represents the mobility of the charges in the doped layer. Equation (2) describes a linear drift velocity for the memristor where the charges migrate at the same rate regardless of the position of the barrier between the layers. A more accurate model is described in [4] where a non-linear drift velocity is introduced, velocity now changes based on position of the barrier between the doped and undoped layers. The drift velocity should be at a maximum when the barrier between the layers is in the middle of the device, and zero when the position of the barrier is at either end [4]. Joglekar proposed equation (3), a window function that is used to achieve the desired velocity based on barrier position.

$$ F \left( \frac{w(t)}{D} \right) = 1 - \left( 2 \left( \frac{w(t)}{D} \right) - 1 \right)^{2p} $$  \hspace{1cm} (3)
where \( p \) is a positive integer that controls the intensity at which the function drives velocity to zero at either end of the device.

Similarly, Biolek proposed another window function in [5] to produce the same effect with a slightly different shape using equation (4):

\[
F \left( \frac{w(t)}{D} \right) = 1 - \left( \frac{w(t)}{D} - stp(-l) \right)^{2p}
\]

(4)

where

\[
stp(l) = \begin{cases} 
1 & \text{if } l > 0 \\
0 & \text{if } l < 0 
\end{cases}
\]

and \( l \) is the current through the memristor. Equation (5) shows the drift velocity definition with the addition of a window function [4-6].

\[
\frac{dw}{dt} = v_D = \frac{\eta \mu_p R_{ON}}{D} I(t) F \left( \frac{w(t)}{D} \right)
\]

(5)

Recall that equation (1) is a function of \( w(t) \) that relates voltage to current. So the complex relationship shown in equation (5) must be solved in terms of \( w(t) \) to provide a current-voltage relationship. A numerical time step solution was developed in [6] to generate a solution for the current in the memristor based on input voltage. This can be seen in equations (6) to (9).

\[
M(w(t_i)) = R_{ON} \frac{w(t_i)}{D} + R_{OFF} \left( 1 - \frac{w(t_i)}{D} \right)
\]

(6)

\[
I(t_{i+1}) = \frac{Q(t_{i+1})}{M(w(t_i))}
\]

(7)

\[
v_D(t_{i+1}) = \frac{\eta \mu_p R_{ON}}{D} I(t_{i+1}) F_p \left( \frac{w(t_i)}{D} \right)
\]

(8)

\[
w(t_{i+1}) = v_D(t_{i+1}) [t_{i+1} - t_i] + w(t_i)
\]

(9)

In this system of equations, \( M(w(t = 0)) \) can be calculated assuming \( w(t = 0) \) is a known value, which represents the initial thickness of the doped layer. It will also be assumed that \( v_D(t = 0) = 0 \), since no charges in the device are moving when there is no voltage applied. The next section discusses the implementation of the memristor models in MATLAB.

### 3. SIMULATION SETUP

Existing studies of these models have utilized sinusoidal inputs to examine if the output has a characteristic hysteresis seen in memristors. Unfortunately such inputs cannot be used to examine the number of resistance levels. Therefore, this study focuses on the application of successive positive voltage sweeps to determine the number of different resistive states that can be achieved in the devices. The applied voltage is in the form of a triangular wave that oscillates between zero and a peak voltage in the range of .25V to 2V. The initial thickness of the oxygen deficient layer is set to be 0.2\( D \) for all of the simulations. This is done to provide more room for \( w(t) \) to increase while remaining conscious of the fact that a value any lower may produce results for an unrealistic fabrication. Lastly, \( \eta \) is set equal to 1 for all of the following simulations.

In the tests conducted, MATLAB was used to test the linear drift model as well as each of the models using window function to produce non-linear drift. The next section discusses the results obtained when comparing the models.
4. SIMULATION RESULTS

The simulation results discussed in this section first show characterization information based on the triangular voltage input signal for each of the three models. The three models are considered to be the linear drift model, Joglekar’s non-linear drift model, and Biolek’s non-linear drift model. Then, as a way to provide theoretical information about the number of resistance states obtainable, simulations were carried out that display a relationship between device thicknesses, the ratio $R_{OFF}/R_{ON}$, and the number of achievable resistance states.

The results for the characterization plots of the linear model are shown in Figure 1. The plot on the top left shows the voltage and current waveforms for the simulation. The current increases with every triangle pulse that is applied to the device, and this is the intuitive result as the plot on the bottom right shows that the resistance drops with each pulse applied. The top right plot shows the I-V characteristic for this simulation. There is a separate hysteresis loop for each pulse since the variable $w(t)$ is at a different position at the beginning of each period of the voltage input. When considering the response of the device when a sine wave is applied, the net charge through the device is zero at the end of each period. This causes the variable $w(t)$ to be periodic with an overlapping hysteresis for multiple periods. It can also be seen in Figure 1 that the size of the hysteresis increases with each period of the voltage waveform. This is mirrored in the voltage and current waveforms where each current pulse grows at an exponential rate. The plot on the bottom left shows the thickness of the doped layer over time as a ratio to the total thickness of the device. It is seen that the doped layer has expanded due to the voltage applied.

![Figure 1](image1.png)

Figure 1. Simulation results for testing linear drift velocity model. Top left shows the current and voltage waveforms with respect to time, and the top right plot shows the I-V characteristic. The bottom left plot shows position of the barrier between the titanium oxide layers and the bottom right plot shows resistance as a function of time. Simulation parameters are, $R_{ON}=100\Omega$, $R_{OFF}=1000\Omega$, $D=46\text{nm}$, $\mu_D=10^{-14}\text{m}^2\text{V}^{-1}\text{s}^{-1}$, $w_0/D=.2$, with a triangle voltage input where $f=2\text{Hz}$ and $A=.25\text{V}$.

Figure 2 provides the simulation results when the non-linear drift velocity is defined by Joglekar’s window function with $p = 1$. A low value for $p$ was chosen because this limits the last hysteresis loop from increasing dramatically. The current and voltage waveforms can be seen in the upper left; they look similar to the linear device, except that the exponential increase in current reduces between the last two pulses. The hysteresis in the I-V curve on the right shows that the widest loop is now in the middle where the window function is a maximum. The plots for $w(t)$ and the resistance also look similar to Figure 1, but they have a smoother decay as the window function is affecting the drift velocity near the edges of the device.
Figure 2. Simulation results for testing the Joglekar non-linear drift velocity model with $p=1$. Top left shows the current and voltage waveforms with respect to time, and the top right plot shows the I-V characteristic. The bottom left plot shows position of the barrier between the titanium oxide layers and the bottom right plot shows resistance as a function of time. Simulation parameters are, $R_{\text{ON}}=100\, \Omega$, $R_{\text{OFF}}=1000\, \Omega$, $D=37\, \text{nm}$, $\mu_{D}=10^{-14}\, \text{m}^2\text{V}^{-1}\text{s}^{-1}$, $w_0/D=0.2$, with a triangle voltage input where $f=2\, \text{Hz}$ and $A=0.25\, \text{V}$.

Figure 3. Simulation results for testing the Biolek non-linear drift velocity model with $p=1$. Top left shows the current and voltage waveforms with respect to time, and the top right plot shows the I-V characteristic. The bottom left plot shows position of the barrier between the titanium oxide layers and the bottom right plot shows resistance as a function of time. Simulation parameters are, $R_{\text{ON}}=100\, \Omega$, $R_{\text{OFF}}=1000\, \Omega$, $D=32\, \text{nm}$, $\mu_{D}=10^{-14}\, \text{m}^2\text{V}^{-1}\text{s}^{-1}$, $w_0/D=0.2$, with a triangle voltage input where $f=2\, \text{Hz}$ and $A=0.25\, \text{V}$.

Figure 3 shows the test results when the drift velocity has non-linearity induced by Biolek’s window function. The results look very similar to the data in Figure 2, except that the window function has a slightly stronger effect. The value for $D$ was set to $32\, \text{nm}$ for this test as opposed to $37\, \text{nm}$ when using Joglekar’s window function. The total thickness of the device was reduced slightly to provide an increase in the memory effect to compensate for the additional reduction provided by the stronger window function.

When implementing a neuromorphic circuit, it is necessary to know how many different resistance levels are available in a given memristor device. The models that have been discussed were used to generate data that predicts the number of resistance states available in a device based on different device parameters. Since this is an analog device, the definition of a resistance level will not be an on/off relationship. Additionally, the exponential nature of the resistance drop must be considered when defining a level. The amplitude and frequency of the input voltage will also have an effect the number of levels; these however were held constant in the experiments to isolate how device parameters determine the resistance levels available in the device.

Since the resistance drop is not constant, a resistance level has been defined as any state change in $w(t)$ that causes a sufficient increase in current upon the application of a single voltage pulse. The sufficient increase in current will be given as a percentage increase from the previous current pulse. When looking at the current and voltage waveforms in
Figure 3, it can be seen that the first four pulses hardly change the device state, and the last four pulses have a much larger impact. The tolerance percentage will decide at what value of $w(t)$ the resistance level changes upon a single voltage pulse.

Figure 4 shows the data collected for testing the linear drift model. The plot on the left shows the number of resistance levels available as a function of device thickness when the ratio $R_{OFF}/R_{ON} = 10$. The plot on the right shows the same data when $R_{OFF}/R_{ON} = 50$. For each plot, the starting thickness was chosen by finding the minimum whole nanometer thickness where $w(t)/D < 1$. In Figure 4 it can be seen that tolerances of 5%, 10%, and 15% were considered as three separate tolerance levels for the increase in peak value for current. This data relates to the uniformity at which the devices are fabricated. If all of the memristor devices in a system are very uniform then a smaller current peak differential is required because the same magnitude voltage pulse is likely to change the resistance of all the devices by the same amount. If non-uniform devices are fabricated, a larger gap is needed between resistance levels because internal resistance may change dramatically from one device to the next.

Figure 4. Plot on the left shows number of resistance levels achieved using the linear drift model for $D=90-115$nm where $R_{ON}/R_{OFF}=10$ for current pulse differentials given as 5, 10, and 15%. Plot on the right shows same data for $R_{ON}/R_{OFF}=50$ and $D=42-55$nm. Other simulation parameters are, $R_{ON}=100\Omega$, $\mu_D=10^{-13}m^2V^{-1}s^{-1}$, $w/D=.2$, with a triangle voltage input where $f=4$Hz and $A=2$V.

Figure 5 shows the resistance level results for the simulation when using Joglekar’s non-linear drift model. The main difference here is that the number of levels increases initially before the expected decay. This is because at these small thicknesses, the memristive effect is so small that very few pulses are needed to drive $w(t)$ to $D$. Once $w(t)$ reaches this limit, a negative pulse must be applied or the device will remain in this state as a linear resistor. The data in Figure 6 shows the simulation results for a case where $w(t)$ approaches $D$ so quickly that the number of resistance levels is reduced. The bottom left plot in Figure 6 shows that after about 1.75s, there is no more room for the oxygen deficient layer to expand and the memristor starts to act as a linear resistor. At this time, the current no longer increases as a function of input pulse and the I-V characteristic becomes a straight line with slope equal to $1/R_{ON}$. Figure 5 shows that when the device thickness is less than 65nm, this effect occurs as the number of resistance levels decreases as device thickness decreases.

Lastly, Figure 7 shows the resistance level data collected for the Biolek window function. The results are similar to the Joglekar model but again the device thickness is reduced as in the results shown in Figures 2 and 3. Since the window function for the Biolek model has a greater effect on drift velocity, the maximum number of resistance levels occurs at a lower device thickness.
Figure 5. Plot on the left shows number of resistance levels achieved using the Joglekar non-linear drift model for $D=60-120\text{nm}$ where $R_{\text{ON}}/R_{\text{OFF}}=10$ for current pulse differentials given as 5, 10, and 15%. Plot on the right shows same data for $R_{\text{ON}}/R_{\text{OFF}}=50$ and $D=30-50\text{nm}$. Other simulation parameters are, $R_{\text{ON}}=100\Omega$, $\mu_D=10^{-12}\text{m}^2\text{V}^{-1}\text{s}^{-1}$, $w_0/D=.2$, with a triangle voltage input where $f=4\text{Hz}$ and $A=2\text{V}$.

Figure 6. Simulation results for testing the Joglekar non-linear drift velocity model with $p=1$. Top left shows the current and voltage waveforms w. r. t. time, and the top right plot shows the I-V characteristic. The bottom left plot shows position of the barrier between the titanium oxide layers and the bottom right plot shows resistance as a function of time. Due to the strong memristive effect, device operates as a linear resistor after 1.5s. Simulation parameters are, $R_{\text{ON}}=100\Omega$, $R_{\text{OFF}}=1000\Omega$, $D=50\text{nm}$, $\mu_D=10^{-14}\text{m}^2\text{V}^{-1}\text{s}^{-1}$, $w_0/D=.2$, with a triangle voltage input where $f=4\text{Hz}$ and $A=2\text{V}$.

Figure 7. Plot on the left shows number of resistance levels achieved using the Biolek non-linear drift model for $D=50-110\text{nm}$ where $R_{\text{ON}}/R_{\text{OFF}}=10$ for current pulse differentials given as 5, 10, and 15%. Plot on the right shows same data for $R_{\text{ON}}/R_{\text{OFF}}=50$ and $D=30-50\text{nm}$. Other simulation parameters are, $R_{\text{ON}}=100\Omega$, $\mu_D=10^{-14}\text{m}^2\text{V}^{-1}\text{s}^{-1}$, $w_0/D=.2$, with a triangle voltage input where $f=4\text{Hz}$ and $A=2\text{V}$. 
5. DISCUSSION

When comparing the number of resistance levels available for the three models, it can be seen that the two non-linear models provide similar results. Figure 8 shows the results for all three models with a pulse differential of 5%. The Biolek and Joglekar models show a similar pattern in the number of resistance levels, but the Biolek model on average provides about one more level relative to device thickness. The capability of the linear model suffers because it will immediately turn into a linear resistor when \( w(t) > D \), and it will not operate in the range where the non-linear models provide the maximum number of resistance levels. In the range the linear model operates correctly, it fits the pattern of the non-linear models and provides a slight increase in the number of resistance levels.

Looking at the characterization plots, it can be seen that hysteresis size increases exponentially with each pulse applied to the device. This is because the resistance drop is linear with respect to the thickness of the doped layer. When the current is calculated using equation (1), it is inversely proportional to the resistance value producing an asymptotic increase as \( w(t) \) approaches \( D \). This is displayed in Figure 9; as the conductance of the memristor increases asymptotically, the doped layer becomes very small. Since this occurs very close to one of the boundaries in the memristor, the window functions described in \([4, 5]\) reduce this effect.

When comparing these results to the experimental results in \([7, 8]\), it can be seen that the exponential increase in hysteresis and current peak is not present in fabricated memristor devices. The hysteresis is initially large, and then diminishes with each pulse. In addition, it was shown in \([8]\) that the current pulses increase logarithmically with each voltage pulse as opposed to exponential.

The method for determining the number of resistance levels described in this paper can still be used since there is still non-linear increase in current. Thus applying this technique to the device described in \([8]\) will show that higher differential current pulses occur when \( w(t) \) is closer to 0 as opposed to when \( w(t) \) approaches \( D \).

Figure 8. Comparison of results for resistance level data presented in previous section using a minimum pulse differential of 5%.

Figure 9. Device conductance as a function of doped layer thickness when using simulations based on equation (1).
6. CONCLUSION

Comparing the results from all three models in Figure 8, it can be seen that the linear model cannot operate in the range where the non-linear models provide the maximum number of resistance levels. Also, the Biolek model provides a slightly higher number of levels than the Joglekar model. When looking at the linear model in its defined region, it provides more resistance levels on average, but it does not provide the maximum number of levels. In all three cases, increasing the ratio \( R_{OFF}/R_{ON} \) reduces the thickness where the maximum number of resistance levels is observed.

Looking at the resistance level data, an argument could be made stating that much of the functionality of the memristor is wasted in the areas where the current peak differential is low. Furthermore, several pulses could be used to change the resistance state in less sensitive areas to increase the number of resistance levels. This would require a more complex circuit that would apply a different number or size of voltage pulses dependant on state. As an alternative for increasing the amount of resistance levels available, circuit designs will be examined in the future that use multiple memristors to model a single synapse.

When comparing these simulations to actual memristor devices fabricated, there is a discrepancy in the I-V characteristics in the form of an incorrectly shaped hysteresis. The window functions that were implemented reduce this effect in the extreme case where \( w(t) \) is close to the boundaries, but an exponential increase can still be seen.

Finally, the resistance of the fabricated devices in [7, 8] appear to change with respect to the magnitude of the voltage input. This information suggests that the metal insulator metal (MIM) structure of memristors may introduce a dynamic resistance component dependant on magnitude of voltage input. Future work includes developing a more advanced model to describe memristor devices with a dynamic resistance component.

REFERENCES